

SN54ALVTH32373, SN74ALVTH32373 2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCES322A – FEBRUARY 2000 – REVISED APRIL 2000

- State-of-the-Art Advanced BiCMOS Technology (ABT) *Widebus+*™ Design for 2.5-V and 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- High Drive ($-24/24$ mA at 2.5-V and $-32/64$ mA at 3.3-V V_{CC})
- I_{off} and Power-Up 3-State Support Hot Insertion
- Use Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating
- Auto3-State Eliminates Bus Current Loading When Output Exceeds $V_{CC} + 0.5$ V
- Flow-Through Architecture Facilitates Printed Circuit Board Layout
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Packaged in Plastic Fine-Pitch Ball Grid Array Package

NOTE: For tape and reel order entry:
The GKER package is abbreviated to KR.

description

The 'ALVTH32373 devices are 32-bit transparent D-type latches with 3-state outputs designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as four 8-bit latches, two 16-bit latches, or one 32-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

When V_{CC} is between 0 and 1.2 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus+ is a trademark of Texas Instruments.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



Copyright © 2000, Texas Instruments Incorporated

SN54ALVTH32373, SN74ALVTH32373

2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCES322A – FEBRUARY 2000 – REVISED APRIL 2000

description (continued)

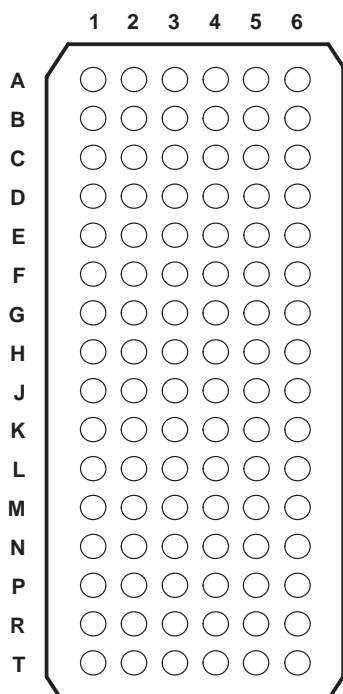
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ALVTH32373 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALVTH32373 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 8-bit latch)

INPUTS			OUTPUT
$\overline{\text{OE}}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

GKE PACKAGE
(TOP VIEW)



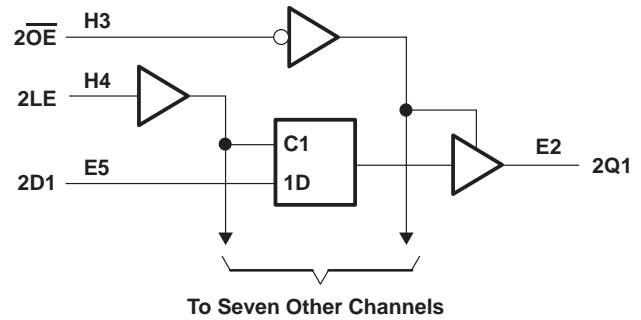
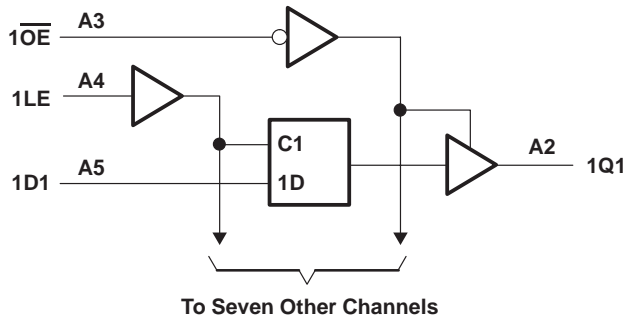
terminal assignments

	1	2	3	4	5	6
A	1Q2	1Q1	$1\overline{\text{OE}}$	1LE	1D1	1D2
B	1Q4	1Q3	GND	GND	1D3	1D4
C	1Q6	1Q5	$1V_{CC}$	$1V_{CC}$	1D5	1D6
D	1Q8	1Q7	GND	GND	1D7	1D8
E	2Q2	2Q1	GND	GND	2D1	2D2
F	2Q4	2Q3	$1V_{CC}$	$1V_{CC}$	2D3	2D4
G	2Q6	2Q5	GND	GND	2D5	2D6
H	2Q7	2Q8	$2\overline{\text{OE}}$	2LE	2D8	2D7
J	3Q2	3Q1	$3\overline{\text{OE}}$	3LE	3D1	3D2
K	3Q4	3Q3	GND	GND	3D3	3D4
L	3Q6	3Q5	$2V_{CC}$	$2V_{CC}$	3D5	3D6
M	3Q8	3Q7	GND	GND	3D7	3D8
N	4Q2	4Q1	GND	GND	4D1	4D2
P	4Q4	4Q3	$2V_{CC}$	$2V_{CC}$	4D3	4D4
R	4Q6	4Q5	GND	GND	4D5	4D6
T	4Q7	4Q8	$4\overline{\text{OE}}$	4LE	4D8	4D7

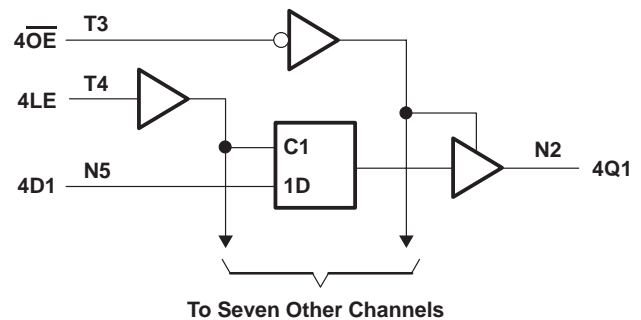
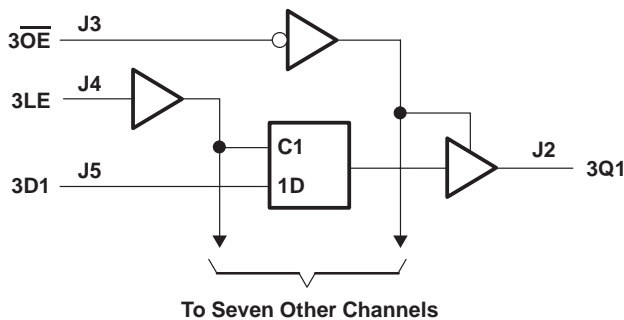
SN54ALVTH32373, SN74ALVTH32373 2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCES322A – FEBRUARY 2000 – REVISED APRIL 2000

logic diagram (positive logic)



NOTE A: $1V_{CC}$ is associated with these channels.



NOTE B: $2V_{CC}$ is associated with these channels.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to 7 V
Output current in the low state, I_O : SN54ALVTH32373	96 mA
SN74ALVTH32373	128 mA
Output current in the high state, I_O : SN54ALVTH32373	-48 mA
SN74ALVTH32373	-64 mA
Continuous current through V_{CC} or GND	± 100 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2)	40°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

SN54ALVTH32373, SN74ALVTH32373

2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCES322A – FEBRUARY 2000 – REVISED APRIL 2000

recommended operating conditions, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (see Note 3)

		SN54ALVTH32373			SN74ALVTH32373			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	2.3		2.7	2.3		2.7	V
V_{IH}	High-level input voltage	1.7			1.7			V
V_{IL}	Low-level input voltage			0.7			0.7	V
V_I	Input voltage	0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current			-6			-8	mA
I_{OL}	Low-level output current			6			8	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1\text{ kHz}$			18			24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
T_A	Operating free-air temperature	-55		125	-40		85	$^{\circ}\text{C}$

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (see Note 3)

		SN54ALVTH32373			SN74ALVTH32373			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	3		3.6	3		3.6	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current			-24			-32	mA
I_{OL}	Low-level output current			24			32	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1\text{ kHz}$			48			64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
T_A	Operating free-air temperature	-55		125	-40		85	$^{\circ}\text{C}$

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ALVTH32373, SN74ALVTH32373 2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCES322A – FEBRUARY 2000 – REVISED APRIL 2000

**electrical characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	SN54ALVTH32373			SN74ALVTH32373			UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{IK}		V _{CC} = 2.3 V, I _I = -18 mA	-1.2			-1.2			V	
V _{OH}		V _{CC} = 2.3 V to 2.7 V, I _{OH} = -100 μA	V _{CC} -0.2			V _{CC} -0.2			V	
		V _{CC} = 2.3 V, I _{OH} = -6 mA	1.8			1.8				
V _{OL}		V _{CC} = 2.3 V to 2.7 V, I _{OL} = 100 μA	0.2						0.2	
		V _{CC} = 2.3 V	I _{OL} = 6 mA	0.4			0.4			
			I _{OL} = 8 mA	0.5						
			I _{OL} = 18 mA							
		I _{OL} = 24 mA	0.5			0.5				
I _I	Control inputs	V _{CC} = 2.7 V, V _I = V _{CC} or GND	±1			±1			μA	
		V _{CC} = 0 or 2.7 V, V _I = 5.5 V	10			10				
	Data inputs	V _{CC} = 2.7 V	V _I = 5.5 V	10			10			
			V _I = V _{CC}	1			1			
		V _I = 0	-5			-5				
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100			μA	
I _{BHL} ‡		V _{CC} = 2.3 V, V _I = 0.7 V	115*			115			μA	
I _{BHH} §		V _{CC} = 2.3 V, V _I = 1.7 V	-10*			-10			μA	
I _{BHLO} ¶		V _{CC} = 2.7 V, V _I = 0 to V _{CC}	300*			300			μA	
I _{BHHO} #		V _{CC} = 2.7 V, V _I = 0 to V _{CC}	-300*			-300			μA	
I _{EX}		V _{CC} = 2.3 V, V _O = 5.5 V	125			125			μA	
I _{OZ(PU/PD)} *		V _{CC} ≤ 1.2 V, V _O = 0.5 V to V _{CC} , V _I = GND or V _{CC} , \overline{OE} = don't care	±100			±100			μA	
I _{OZH}		V _{CC} = 2.7 V, V _O = 2.3 V, V _I = 0.7 V or 1.7 V	5			5			μA	
I _{OZL}		V _{CC} = 2.7 V, V _O = 0.5 V, V _I = 0.7 V or 1.7 V	-5			-5			μA	
I _{CC}		V _{CC} = 2.7 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	0.04	0.1	0.04	0.1	mA		
			Outputs low	2.3	4.5	2.3	4.5			
			Outputs disabled	0.04	0.1	0.04	0.1			
C _i		V _{CC} = 2.5 V, V _I = 2.5 V or 0	3.5			3.5			pF	
C _o		V _{CC} = 2.5 V, V _O = 2.5 V or 0	6			6			pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 2.5 V, T_A = 25°C.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

¶ An external driver must source at least I_{BHLO} to switch this node from low to high.

An external driver must sink at least I_{BHHO} to switch this node from high to low.

|| Current into an output in the high state when V_O > V_{CC}

* High-impedance state during power up or power down

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ALVTH32373, SN74ALVTH32373

2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCES322A – FEBRUARY 2000 – REVISED APRIL 2000

electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALVTH32373			SN74ALVTH32373			UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX		
V_{IK}	$V_{CC} = 3\text{ V}$, $I_I = -18\text{ mA}$		-1.2			-1.2			V	
V_{OH}	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$			$V_{CC}-0.2$			V	
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2							
			$I_{OH} = -32\text{ mA}$				2			
V_{OL}	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$		0.2			0.2			V	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$				0.4				
		$I_{OL} = 24\text{ mA}$	0.5							
		$I_{OL} = 32\text{ mA}$				0.5				
		$I_{OL} = 48\text{ mA}$	0.55							
		$I_{OL} = 64\text{ mA}$				0.55				
I_I	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND	± 1			± 1			μA	
		$V_{CC} = 0$ or 3.6 V , $V_I = 5.5\text{ V}$	10			10				
	Data inputs	$V_{CC} = 3.6\text{ V}$	$V_I = 5.5\text{ V}$	10			10			
			$V_I = V_{CC}$	1			1			
		$V_I = 0$	-5			-5				
I_{off}	$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V					± 100			μA	
I_{BHL}^\ddagger	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$		75*			75			μA	
I_{BHH}^\S	$V_{CC} = 3\text{ V}$, $V_I = 2\text{ V}$		-75*			-75			μA	
I_{BHLO}^\P	$V_{CC} = 3.6\text{ V}$, $V_I = 0$ to V_{CC}		500*			500			μA	
$I_{BHHO}^\#$	$V_{CC} = 3.6\text{ V}$, $V_I = 0$ to V_{CC}		-500*			-500			μA	
I_{EX}^\parallel	$V_{CC} = 3\text{ V}$, $V_O = 5.5\text{ V}$		125			125			μA	
$I_{OZ(PU/PD)}^*$	$V_{CC} \leq 1.2\text{ V}$, $V_O = 0.5\text{ V to } V_{CC}$, $V_I = \text{GND or } V_{CC}$, $\overline{OE} = \text{don't care}$		± 100			± 100			μA	
I_{OZH}	$V_{CC} = 3.6\text{ V}$	$V_O = 3\text{ V}$, $V_I = 0.8\text{ V or } 2\text{ V}$	5			5			μA	
I_{OZL}	$V_{CC} = 3.6\text{ V}$	$V_O = 0.5\text{ V}$, $V_I = 0.8\text{ V or } 2\text{ V}$	-5			-5			μA	
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND		Outputs high	0.07	0.1	0.07	0.1	mA		
			Outputs low	3.2	5	3.2	5			
			Outputs disabled	0.07	0.1	0.07	0.1			
ΔI_{CC}^\square	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND		0.4			0.4			mA	
C_i	$V_{CC} = 3.3\text{ V}$, $V_I = 3.3\text{ V or } 0$		3.5			3.5			pF	
C_o	$V_{CC} = 3.3\text{ V}$, $V_O = 3.3\text{ V or } 0$		6			6			pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

¶ An external driver must source at least I_{BHLO} to switch this node from low to high.

An external driver must sink at least I_{BHHO} to switch this node from high to low.

|| Current into an output in the high state when $V_O > V_{CC}$

* High-impedance state during power up or power down

□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ALVTH32373, SN74ALVTH32373
2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCES322A – FEBRUARY 2000 – REVISED APRIL 2000

timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

		SN54ALVTH32373		SN74ALVTH32373		UNIT
		MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	1.5		1.5		ns
t_{su}	Setup time, data before LE↓	Data high	1.1	1		ns
		Data low	1.6	1.5		
t_h	Hold time, data after LE↓	Data high	1	0.9		ns
		Data low	1.6	1.5		

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 2)

		SN54ALVTH32373		SN74ALVTH32373		UNIT
		MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	1.5		1.5		ns
t_{su}	Setup time, data before LE↓	Data high	1.5	1.4		ns
		Data low	1.6	0.9		
t_h	Hold time, data after LE↓	Data high	1	0.9		ns
		Data low	1.5	1.4		

switching characteristics over recommended operating free-air temperature range, $C_L = 30\text{ pF}$, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH32373		SN74ALVTH32373		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	3.4	1	3.3	ns
t_{PHL}			1	4.3	1	4.2	
t_{PLH}	LE	Q	1.4	3.9	1.5	3.8	ns
t_{PHL}			1.4	4.6	1.5	4.5	
t_{PZH}	\overline{OE}	Q	1.7	4.4	1.8	4.3	ns
t_{PZL}			1.4	4.1	1.5	4	
t_{PHZ}	\overline{OE}	Q	1.4	4.7	1.5	4.6	ns
t_{PLZ}			1	3.7	1	3.6	

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH32373		SN74ALVTH32373		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	3.2	1	3.1	ns
t_{PHL}			1	3.4	1	3.3	
t_{PLH}	LE	Q	1	3.4	1	3.3	ns
t_{PHL}			1	3.6	1	3.5	
t_{PZH}	\overline{OE}	Q	1.3	4.1	1.4	4	ns
t_{PZL}			1	3.5	1	3.4	
t_{PHZ}	\overline{OE}	Q	1.4	5	1.5	4.9	ns
t_{PLZ}			1.4	4.6	1.5	4.5	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

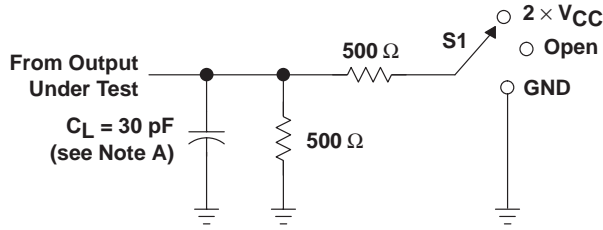


SN54ALVTH32373, SN74ALVTH32373
2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCES322A – FEBRUARY 2000 – REVISED APRIL 2000

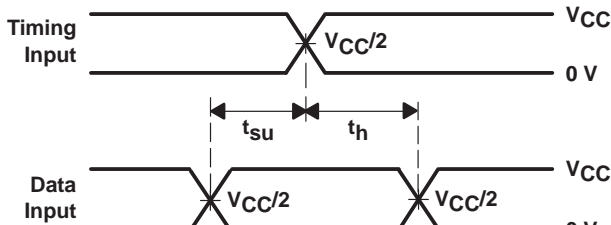
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

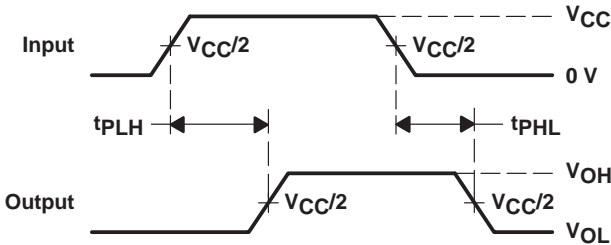


LOAD CIRCUIT

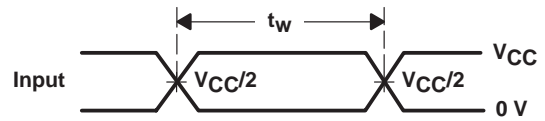
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



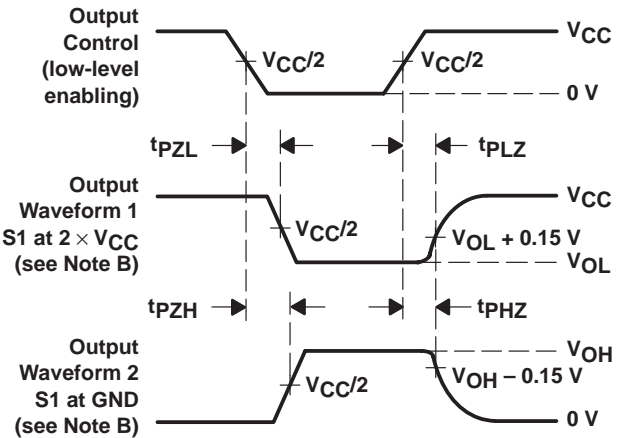
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

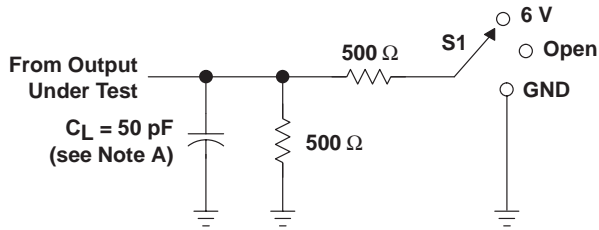
Figure 1. Load Circuit and Voltage Waveforms

SN54ALVTH32373, SN74ALVTH32373
2.5-V/3.3-V 32-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCES322A – FEBRUARY 2000 – REVISED APRIL 2000

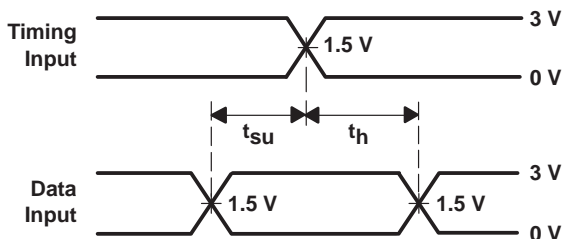
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

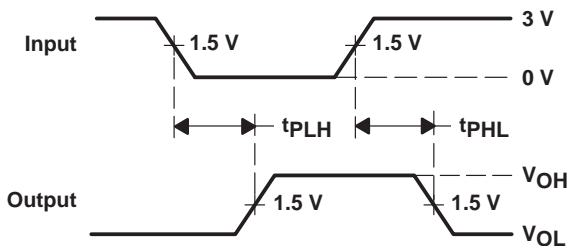


LOAD CIRCUIT

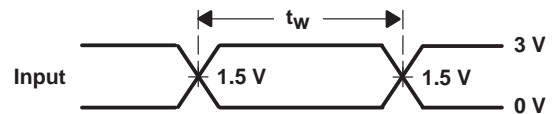
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



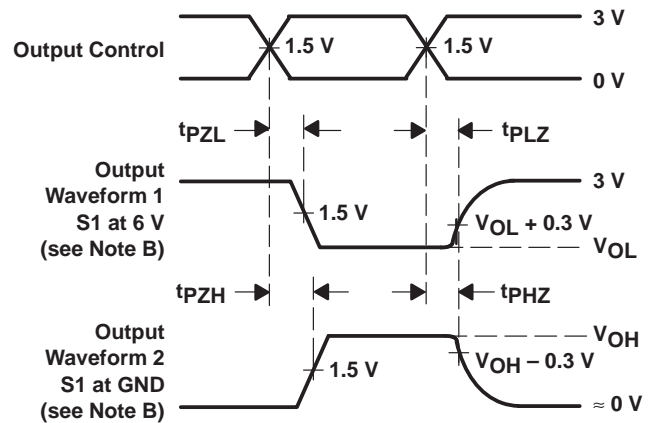
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVTH32373ZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
SN74ALVTH32373KR	NRND	LFBGA	GKE	96	1000	TBD	SNPB	Level-2-235C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ALVTH32373ZKER	LFBGA	ZKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1
SN74ALVTH32373KR	LFBGA	GKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

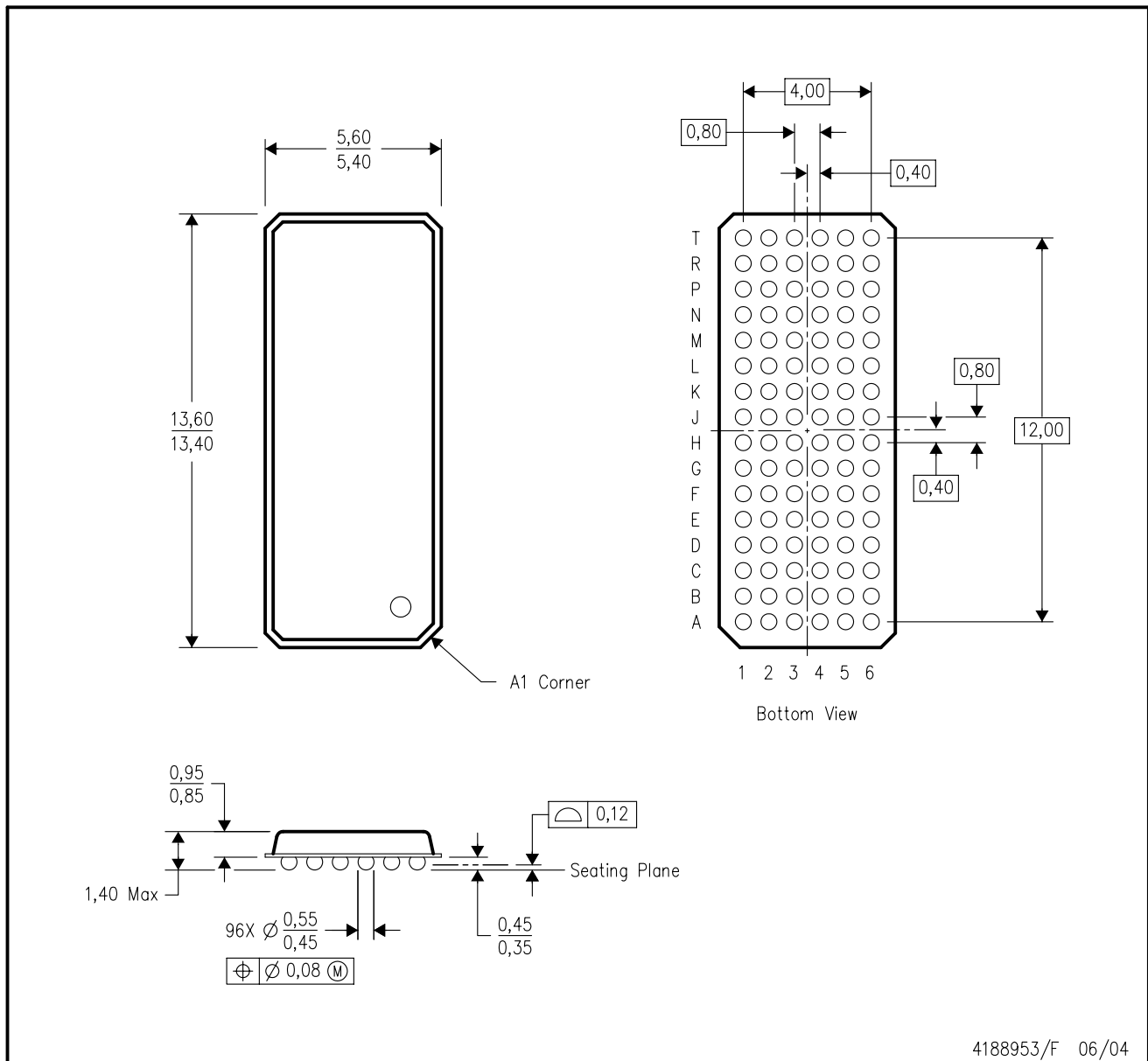


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ALVTH32373ZKER	LFBGA	ZKE	96	1000	346.0	346.0	41.0
SN74ALVTH32373KR	LFBGA	GKE	96	1000	346.0	346.0	41.0

GKE (R-PBGA-N96)

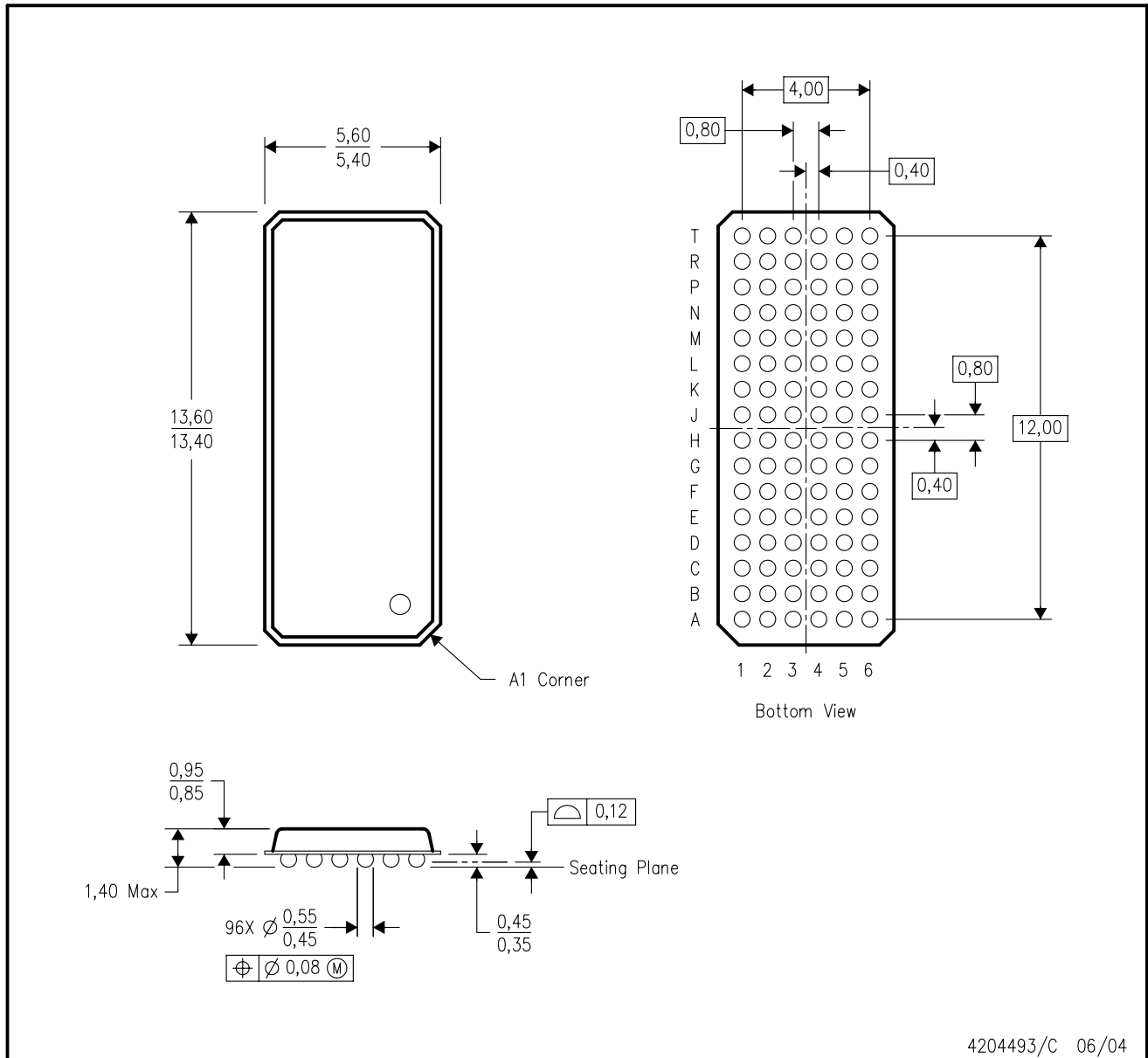
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation CC.
 - D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation CC.
 - D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated